

AMENDMENTIn the Claims

- 1  
2 1 (original): A receiver, in a digital transmission system, comprising a channel decoder for  
3 protecting a transmitted signal against channel transmission errors, the channel decoder  
4 comprising:  
5 - a set of co-processors including at least 3 clusters of programmable co-processors  
6 for executing the functions of a digital front-end block (DFE), a channel correction block (CCIN)  
7 and a forward error correction block (FEC), respectively,  
8 - a general purpose processor (DSP) for managing control, synchronization and  
9 configuration of the channel decoder, and  
10 - a memory (SM) shared between the clusters and the general purpose processor.
- 1 2 (original): A receiver as claimed in claim 1, wherein the set of co-processors comprises:  
2 - a digital front-end processor (DFE) for computing:  
3 • base-band demodulation of the received signal,  
4 • a programmable Nyquist filter,  
5 and for controlling an automatic gain control loop (AGC) and synchronization loops for time and  
6 carrier recovery,  
7 - a fast Fourier transform processor (FFT) for performing demodulation in the case of  
8 multi-carrier systems and frequency domain equalization in the case of mono-carrier systems,  
9 - an adaptive filter array processor (AFA) for time domain equalization, interference  
10 rejection and frequency interpolation in the case of COFDM modulation,  
11 - a forward error correction processor (FEC) for decoding Reed-Solomon and  
12 convolutional codes which were used during transmission.

3 (original): A broadcasting system comprising a receiver and a transmitter, in a digital video transmission system, wherein the receiver is according to any one of claim 1.

Serial No. 09/982,267

2

13 4 (original): In a digital video receiver, a method of channel decoding for protecting a  
14 transmitted signal against transmission errors, the method comprising the steps of base-band  
15 demodulation, channel correction and forward error correction of the received signal, each step  
16 being performed by a cluster of programmable co-processors, a general purpose processor with a  
17 shared memory being provided for managing control, synchronization and configuration of said  
18 clusters of co-processors.

1 5 (previously presented): A computer program product for a receiver comprising a set of  
2 instructions which, when loaded into the receiver, causes the receiver to carry out the method as  
3 claimed in claim 4.

1 6 (previously presented): A signal for carrying a computer program, the computer program  
2 being arranged to cause a programmable device to carry out steps comprising: base-band  
3 demodulation, channel correction and forward error correction of a received digital video signal,  
4 the programmable device comprising a cluster of programmable co-processors for performing  
5 each step, and a general purpose processor with a shared memory for managing control,  
6 synchronization and configuration of said clusters of co-processors.

1 7 (previously presented): The receiver of claim 1, wherein the clusters of co-processors are  
2 programmable to allow for handling a plurality of data formats, and each respective cluster  
3 performs only a single one of the recited three functions.

1 8 (previously presented): The method of claim 4, wherein the clusters of co-processors are  
2 programmable to allow for handling a plurality of data formats, and each respective cluster  
3 performs only a single one of the recited three steps.

1 9 (previously presented): The computer program of claim 5, wherein the clusters of co-  
2 processors are programmable for handling a plurality of data formats, and each respective cluster  
3 performs only a single one of the recited three steps.

1 10 (previously presented): The signal of claim 6, wherein the clusters of co-processors are  
2 programmable for handling a plurality of data formats, and each respective cluster performs only  
3 a single one of the recited three steps.

1 11 (previously presented): A channel decoder for digital video data comprising:  
2     ▪ an input for receiving signals in differing formats;  
3     ▪ at least one first cluster comprising at least one first programmable co-processor for executing  
4 functions of a digital front-end block (DFE), which first cluster is programmable to adapt to  
5 all of the differing formats;  
6     ▪ at least one a second cluster comprising at least one second programmable co-processor for  
7 executing functions of a channel correction block (CHN), which second cluster is  
8 programmable to adapt to all of the differing formats;  
9     ▪ at least one a third cluster comprising at least one third programmable co-processor for  
10 executing functions of a forward error correction block (FEC), which third cluster is  
11 programmable to adapt to all of the differing formats;  
12     ▪ a general purpose processor (DSP) for managing control, synchronization and configuration  
13 of the channel cluster; and  
14     ▪ a memory (SM) shared between the processors.

12 (currently amended): ~~13~~: The decoder of claim 11 ~~12~~, wherein at least one of the processors is implemented in hardware.

13 (currently amended): ~~14~~: The decoder of claim 11 ~~12~~, wherein at least one of the processors is implemented in software.

14 (currently amended): ~~15~~: The decoder of claim 11 ~~12~~, wherein the decoder is adapted to receive a signal carrying a computer program for programming the processors.

15 (currently amended): ~~16~~: The decoder of claim 11 ~~12~~, wherein at least one of the first, second and third programmable co-processors comprises a cluster of co-processors.